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Remarks

Claims 1-3 and 12 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The Office Action dated April 26, 2007 indicated an objection to the abstract and that claims 1-3 stand rejected under 35 U.S.C. § 102(b) over Krivokapic (U.S. Patent 6,339,244).

Regarding the objection to the abstract, Applicant was provided a copy of the abstract (as amended on page 2 of this paper) on a single page as indicated on page 3 of this paper. Thus, Applicant requests that the objection to the abstract be removed.

Applicant respectfully traverses the Section 102(b) rejection of claims 1-3 because the cited portions of the Krivokapic reference do not correspond to claimed limitations directed to the Deep N implant layer being between either the source or drain and the parasitic MOS channel. The Office Action cites to Krivokapic's n-silicon region 40 as allegedly corresponding to the Deep N implant layer of the claimed invention. However, the cited portions of Krivokapic teach that n-silicon region 40 is below the buried insulator layer 14 and that n-silicon region 40 will prevent flow of current from the drain through the buried insulator layer 14 to the source. *See, e.g.,* Figure 5 and Col. 3:24-33. Thus, the cited portions of the Krivokapic reference do not teach that a Deep N implant layer is between either the source or drain and the parasitic MOS channel as in the claimed invention. Accordingly, the Section 102(b) rejection of claim 1, as well as the rejection of claims 2-3 that depend from claim 1, is improper and Applicant requests that it be withdrawn.

Notwithstanding, in an effort to facilitate prosecution, Applicant has amended claim 1 to include an insulator layer that is between the SOI layer and the substrate layer, and to indicate that the Deep N implant layer is between either the source or drain and the insulator layer. As discussed above, the cited portions of the Krivokapic reference teach that buried insulator layer 14 is between the source and drain and the n-silicon region 40 (*see, e.g.,* Figure 5 and Col. 3:24-33), not that the Deep N implant layer is between either the source or drain and the insulator layer as in the claimed invention. Therefore, the

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Section 102(b) rejection of claims 1-3 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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